

## CLAIMS

What is claimed is:

1           1.       A thermal management system for an integrated circuit die, comprising:  
2       a temperature detection element formed directly on said integrated circuit die, said  
3           temperature detection element including at least one temperature sensor having an  
4           output;  
5       a power modulation element formed directly on said integrated circuit die and configured  
6           to reduce power consumption of said integrated circuit die in response to a logical  
7           change in state at said output of said at least one temperature sensor;  
8       a control element formed directly on said integrated circuit die, said control element  
9           including at least one register providing an enable/disable bit for said thermal  
10       management system; and  
11       a visibility element formed directly on said integrated circuit die and configured to  
12       indicate a status of said output of said at least one temperature sensor.

1           2.       The system of claim 1, said at least one temperature sensor comprising:  
2       a reference voltage source providing a reference voltage;  
3       a programmable voltage source providing a programmable voltage proportional to a  
4           temperature of said integrated circuit die; and  
5       a comparator having one input coupled via a first signal line to said reference voltage  
6           source and another input coupled via a second signal line to said programmable  
7           voltage source, said comparator configured to provide said logical change in state  
8           at said output of said at least one temperature sensor in response to said  
9           programmable voltage substantially equaling said reference voltage.

1           3.       The system of claim 2, further comprising a pulse dampener coupled to  
2       said first signal line and configured to at least partially remove electrical noise from said  
3       reference voltage.

1           4.       The system of claim 2, further comprising an analog filter coupled to said  
2 second signal line and said first signal line, said analog filter configured to detect voltage  
3 spikes present in said reference voltage and to add substantially identical voltage spikes  
4 to said programmable voltage.

1           5.       The system of claim 2, further comprising a digital filter coupled to an  
2 output of said comparator, said digital filter including an up-down counter configured to  
3 count clock pulses, said up-down counter configured to increment once for each clock  
4 pulse detected when said comparator output is at a logical high and to decrement once for  
5 each clock pulse detected when said comparator output is at a logical low.

1           6.       The system of claim 1, said control element further including another  
2 register selected from a group consisting of a register configured to selectively disengage  
3 a specified portion of said thermal management system, a register configured to enable  
4 said thermal management system in response to an occurrence of an external event, a  
5 register configured to force said thermal management system active while overriding a  
6 disable bit provided by said at least one register, and a register configured to allow  
7 external software and hardware to enable said thermal management system.

1           7.       The system of claim 1, said visibility element including at least one device  
2 selected from a group consisting of a register configured to indicate said status of said  
3 temperature sensor output, a register providing a sticky bit, a counter configured to count  
4 a number of lost clock cycles resulting from operation of said thermal management  
5 system, and circuitry configured to generate an interrupt when said temperature sensor  
6 output transitions to a different logical state.

1           8.       The system of claim 1, said power modulation element configured to  
2 lower a supply voltage to said integrated circuit die, lower a frequency of a clock signal  
3 provided by internal clock circuitry on said integrated circuit die, perform clock gating of  
4 said clock signal provided by said internal clock circuitry, perform clock throttling of said  
5 clock signal provided by said internal clock circuitry, selectively block clock pulses of  
6 said clock signal provided by said internal clock circuitry, disable at least one of a  
7 plurality of functional units on said integrated circuit die, limit instructions sent to at least  
8 one of said plurality of functional units on said integrated circuit die, or change a  
9 behavior of at least one of said plurality of functional units on said integrated circuit die.

1           9.       A microprocessor, comprising:  
2 a die having a plurality of functional units formed thereon;  
3 internal clock circuitry formed on said die and coupled to at least one of said plurality of  
4 functional units; and  
5 a thermal management system formed directly on said die, comprising:  
6 a temperature detection element including at least one temperature sensor having  
7 an output;  
8 a power modulation element configured to reduce power consumption of at least  
9 one of said functional units in response to a logical change in state at said  
10 output of said at least one temperature sensor;  
11 a control element including at least one register providing an enable/disable bit for  
12 said thermal management system; and  
13 a visibility element configured to indicate a status of said output of said at least  
14 one temperature sensor.

1           10.    The microprocessor of claim 9, said at least one temperature sensor  
2    comprising:  
3    a reference voltage source providing a reference voltage;  
4    a programmable voltage source providing a programmable voltage proportional to a  
5       temperature of said die; and  
6    a comparator having one input coupled via a first signal line to said reference voltage  
7       source and another input coupled via a second signal line to said programmable  
8       voltage source, said comparator configured to provide said logical change in state  
9       at said output of said at least one temperature sensor in response to said  
10      programmable voltage substantially equaling said reference voltage.

1           11.    The microprocessor of claim 10, further comprising a pulse dampener  
2    coupled to said first signal line and configured to at least partially remove electrical noise  
3    from said reference voltage.

1           12.    The microprocessor of claim 10, further comprising an analog filter  
2    coupled to said second signal line and said first signal line, said analog filter configured  
3    to detect voltage spikes present in said reference voltage and to add substantially identical  
4    voltage spikes to said programmable voltage.

1           13.    The microprocessor of claim 10, further comprising a digital filter coupled  
2    to an output of said comparator, said digital filter including an up-down counter  
3    configured to count clock pulses, said up-down counter configured to increment once for  
4    each clock pulse detected when said comparator output is at a logical high and to  
5    decrement once for each clock pulse detected when said comparator output is at a logical  
6    low.

1           14.     The microprocessor of claim 9, said control element further including  
2     another register selected from a group consisting of a register configured to selectively  
3     disengage a specified portion of said thermal management system, a register configured  
4     to enable said thermal management system in response to an occurrence of an external  
5     event, a register configured to force said thermal management system active while  
6     overriding a disable bit provided by said at least one register, and a register configured to  
7     allow external software and hardware to enable said thermal management system.

1           15.     The microprocessor of claim 9, said visibility element including at least  
2     one device selected from a group consisting of a register configured to indicate said status  
3     of said temperature sensor output, a register providing a sticky bit, a counter configured  
4     to count a number of lost clock cycles resulting from operation of said thermal  
5     management system, and circuitry configured to generate an interrupt when said  
6     temperature sensor output transitions to a different logical state.

1           16.     The microprocessor of claim 9, said power modulation element configured  
2     to lower a supply voltage to said die, lower a frequency of a clock signal provided by said  
3     internal clock circuitry, perform clock gating of said clock signal provided by said  
4     internal clock circuitry, perform clock throttling of said clock signal provided by said  
5     internal clock circuitry, selectively block clock pulses of said clock signal provided by  
6     said internal clock circuitry, disable at least one of said plurality of functional units on  
7     said die, limit instructions sent to at least one of said plurality of functional units on said  
8     die, or change a behavior of at least one of said plurality of functional units on said die.

1           17.    A computer system, comprising:  
2    at least one memory device coupled to a bus;  
3    at least one microprocessor coupled to said bus and said at least one memory device, said  
4           at least one microprocessor comprising:  
5           a die having a plurality of functional units formed thereon;  
6           internal clock circuitry formed on said die and coupled to at least one of said  
7           plurality of functional units;  
8           a temperature detection element formed directly on said die, said temperature  
9           detection element including at least one temperature sensor having an  
10          output;  
11          a power modulation element formed directly on said die and configured to reduce  
12          power consumption of at least one of said functional units in response to a  
13          logical change in state at said output of said at least one temperature  
14          sensor;  
15          a control element formed directly on said die, said control element including at  
16          least one register providing an enable/disable bit for said thermal  
17          management system; and  
18          a visibility element formed directly on said die and configured to indicate a status  
19          of said output of said at least one temperature sensor, said temperature  
20          detection, power modulation, control, and visibility elements comprising a  
21          thermal management system for said die.

1        18.    The computer system of claim 17, said at least one temperature sensor  
2 comprising:  
3 a reference voltage source providing a reference voltage;  
4 a programmable voltage source providing a programmable voltage proportional to a  
5 temperature of said die; and  
6 a comparator having one input coupled via a first signal line to said reference voltage  
7 source and another input coupled via a second signal line to said programmable  
8 voltage source, said comparator configured to provide said logical change in state  
9 at said output of said at least one temperature sensor in response to said  
10 programmable voltage substantially equaling said reference voltage.

1        19.    The computer system of claim 18, further comprising a pulse dampener  
2 coupled to said first signal line and configured to at least partially remove electrical noise  
3 from said reference voltage.

1        20.    The computer system of claim 18, further comprising an analog filter  
2 coupled to said second signal line and said first signal line, said analog filter configured  
3 to detect voltage spikes present in said reference voltage and to add substantially identical  
4 voltage spikes to said programmable voltage.

1        21.    The computer system of claim 18, further comprising a digital filter  
2 coupled to an output of said comparator, said digital filter including an up-down counter  
3 configured to count clock pulses, said up-down counter configured to increment once for  
4 each clock pulse detected when said comparator output is at a logical high and to  
5 decrement once for each clock pulse detected when said comparator output is at a logical  
6 low.

1           22.     The computer system of claim 17, said control element further including  
2 another register selected from a group consisting of a register configured to selectively  
3 disengage a specified portion of said thermal management system, a register configured  
4 to enable said thermal management system in response to an occurrence of an external  
5 event, a register configured to force said thermal management system active while  
6 overriding a disable bit provided by said at least one register, and a register configured to  
7 allow external software and hardware to enable said thermal management system.

1           23.     The computer system of claim 17, said visibility element including at least  
2 one device selected from a group consisting of a register configured to indicate said status  
3 of said temperature sensor output, a register providing a sticky bit, a counter configured  
4 to count a number of lost clock cycles resulting from operation of said thermal  
5 management system, and circuitry configured to generate an interrupt when said  
6 temperature sensor output transitions to a different logical state.

1           24.     The computer system of claim 17, said power modulation element  
2 configured to lower a supply voltage to said die, lower a frequency of a clock signal  
3 provided by said internal clock circuitry, perform clock gating of said clock signal  
4 provided by said internal clock circuitry, perform clock throttling of said clock signal  
5 provided by said internal clock circuitry, selectively block clock pulses of said clock  
6 signal provided by said internal clock circuitry, disable at least one of said plurality of  
7 functional units on said die, limit instructions sent to at least one of said plurality of  
8 functional units on said die, or change a behavior of at least one of said plurality of  
9 functional units on said die.



1           25.    A method of performing thermal management on a microprocessor,  
2    comprising:  
3    providing an enable bit to a register of a thermal management system to activate said  
4       thermal management system;  
5    measuring a temperature on a die of said microprocessor with a sensor of said thermal  
6       management system;  
7    providing a logical low at an output of said sensor when said temperature is below a trip  
8       point;  
9    providing a logical high at said sensor output when said temperature equals or exceeds  
10       said trip point;  
11   engaging a power reduction mechanism to reduce power consumption of said die in  
12       response to said logical high at said sensor output; and  
13   providing an indication of a logical status of said output of said sensor to an external  
14       device.

1           26.    The method of claim 25, said engaging a power reduction mechanism  
2    comprising an act selected from a group consisting of lowering a supply voltage to said  
3    die, lowering a frequency of a clock signal provided by internal clock circuitry of said  
4    microprocessor, performing clock gating of said clock signal provided by said internal  
5    clock circuitry, performing clock throttling of said clock signal provided by said internal  
6    clock circuitry, selectively blocking clock pulses of said clock signal provided by said  
7    internal clock circuitry, disabling at least one of a plurality of functional units on said  
8    microprocessor, limiting instructions sent to at least one of said plurality of functional  
9    units on said microprocessor, and changing a behavior of at least one of said plurality of  
10   functional units on said microprocessor.

1           27.    The method of claim 25, said providing an enable bit to a register of said  
2    thermal management system comprising providing an enable bit to said register from an  
3    external operating system.

1           28.    The method of claim 25, further comprising:  
2    engaging said power reduction mechanism for a specified time period;  
3    polling said sensor output after expiration of said specified time period;  
4    engaging said power reduction mechanism for at least another said specified time period  
5           when said sensor output exhibits said logical high; and  
6    halting said power reduction mechanism when said sensor output exhibits said logical  
7           low;

1           29.    The method of claim 25, further comprising:  
2    engaging said power reduction mechanism for a specified time period;  
3    continuously polling said sensor output after expiration of said specified time period; and  
4    halting said power reduction mechanism when said sensor output exhibits said logical  
5           low.

1           30.    The method of claim 25, further comprising:  
2    providing said logical low at said sensor output when said temperature is below an untrip  
3           point, said untrip point less than said trip point; and  
4    halting said power reduction mechanism in response to said logical low.

1           31.    The method of claim 25, further comprising:  
2    coupling an up-down counter to said sensor output;  
3    incrementing said up-down counter once for every clock pulse of said clock signal  
4           provided by said internal clock circuitry when said sensor output exhibits said  
5           logical high; and  
6    decrementing said up-down counter once for every clock pulse of said clock signal  
7           provided by said internal clock circuitry when said sensor output exhibits said  
8           logical low.

1           32.     The method of claim 25, further comprising:  
2     defining a plurality of trip temperatures, a highest of said plurality of trip temperatures  
3           corresponding to said trip point;  
4     assigning a plurality of duty cycle values to said plurality of trip temperatures, one duty  
5           cycle value of said plurality of duty cycle values corresponding to at least one of  
6           said plurality of trip temperatures; and  
7     providing a clock signal from said internal clock circuitry exhibiting said one duty cycle  
8           value in response to said temperature substantially equaling said at least one  
9           corresponding trip temperature.

1           33.     The method of claim 25, further comprising counting a number of clock  
2     cycles eliminated from an output of said internal clock circuitry resulting from said  
3     engaging a power reduction mechanism.

1           34.     An apparatus, comprising:  
2     a temperature detection element, said temperature detection element including at least  
3           one temperature sensor having an output;  
4     a power modulation element, said power modulation element to reduce power  
5           consumption of an integrated circuit die in response to a logical change in state at  
6           said output of said at least one temperature sensor;  
7     a visibility element, said visibility element to indicate a status of said output of said at  
8           least one temperature sensor, said visibility element comprising:  
9           a register to indicate said status of said temperature sensor output;  
10          a register providing a sticky bit;  
11          a counter to count a number of lost clock cycles resulting from operation of said  
12          apparatus; and  
13          circuitry to generate an interrupt when said temperature sensor output transitions  
14          to a different logical state.

1           35.    The apparatus of claim 34, further including a control element, said  
2 control element comprising:  
3 a register providing an enable/disable bit for said apparatus;  
4 a register configured to selectively disengage a specified portion of said apparatus;  
5 a register configured to enable said apparatus in response to an occurrence of an external  
6 event;  
7 a register configured to force said apparatus active while overriding a disable bit provided  
8 at said enable/disable bit; and  
9 a register configured to allow external software and hardware to enable said apparatus.

1           36.    The system of claim 34, said power modulation element configured to  
2 lower a supply voltage to said integrated circuit die, lower a frequency of a clock signal  
3 provided by internal clock circuitry on said integrated circuit die, perform clock gating of  
4 said clock signal provided by said internal clock circuitry, perform clock throttling of said  
5 clock signal provided by said internal clock circuitry, selectively block clock pulses of  
6 said clock signal provided by said internal clock circuitry, disable at least one of a  
7 plurality of functional units on said integrated circuit die, limit instructions sent to at least  
8 one of said plurality of functional units on said integrated circuit die, or change a  
9 behavior of at least one of said plurality of functional units on said integrated circuit die.